Ethernet Controller Data Sheet

Features

The GMAC core has the following features:

- Supports 10/100/1000 Mbps data transfer rates with the following PHY interfaces:
  - IEEE 802.3-compliant GMII/MII (default) interface to communicate with an external Gigabit/Fast Ethernet PHY.
  - IEEE 802.3z-compliant TBI, (optional), with auto-negotiation to communicate with an external PHY.
  - RGMII/RTBI interface (optional) to communicate with an external gigabit PHY.
  - SGMII interface (optional) to communicate with an external gigabit PHY.
  - SMII/RMII interface (optional) to communicate with an external Fast Ethernet PHY.
  - RevMII interface (optional) to directly communicate with a remote MAC.
- Provides the following features for full-duplex operation:
  - IEEE 802.3x flow control automatic transmission of zero-quanta pause frame on flow control input de-assertion.
  - Optional forwarding of received pause control frames to the user application.
- Provides the following features for half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using back-pressure support
  - Frame bursting and frame extension in 1000 Mbps half-duplex operation
- Supports preamble and start-of-frame data (SFD) insertion in Transmit path. In the Receive path, the GMAC core supports preamble and SFD deletion.
- Supports Automatic CRC and pad generation controllable on a per-frame basis. Provides options for Automatic Pad/CRC Stripping on receive frames.
- Supports a variety of flexible address filtering modes such as:
  - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte.
  - Up to 31 48-bit SA address comparison check with masks for each byte.
  - 64-bit Hash filter (optional) for multicast and unicast (DA) addresses.
  - Option to pass all multicast addressed frames.
  - Promiscuous mode support to pass all frames without any filtering for network monitoring.
  - Passes all incoming packets (as per filter) with a status report.
- Supports programmable frame length to support Standard or Jumbo Ethernet frames with up to 16 KB of size.
- Supports programmable Interframe Gap (IFG) (40-96 bit times in steps of 8).
- Supports separate 32-bit status for transmit and receive packets.
- Supports IEEE 802.1Q VLAN tag detection for reception frames.
- Supports separate transmission, reception, and control interfaces to the Application.
- Supports configurable big-endian and little-endian for the Transmit and Receive paths.
- Supports 32/64/128-bit data transfer interface on the system-side.
- Provides the support for network statistics (optional) with RMON/MIB Counters (RFC2819/RFC2665).
- Provides an optional module that you can use for detection of LAN wake-up frames and AMD

Magic Packet frames.

- Provides an optional Receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1).
- Provides an optional Enhanced Receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2).
- Provides an optional module to support Ethernet frame time stamping as described in IEEE 1588-2002 and IEEE 1588-2008. Sixty-four-bit time stamps are given in the transmit or receive status of each frame.
- Supports MDIO Master interface (optional) for PHY device configuration and management.
- Supports the standard IEEE P802.3az, version D2.0 for Energy Efficient Ethernet.

Availability

- Q4, 2010

*To obtain more information about the Ethernet Controller or other C*Core™ products, please contact the C*Core Technology Co., Ltd. by phone: 0512-68091375, email: support@china-core.com or web: http://www.china-core.com.*